**SPICE PROJECT**

**By**

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**Problem Statement**

**Use any SPICE (Simulation Program with Integrated Circuit Emphasis) simulator to answer any one out of three questions. Choose the same technology parameters for all NMOS transistors (similarly for all PMOS transistors) and fix the size of the minimum-sized transistor for all questions, and clearly specify the values that you are using. Make reasonable approximations, if necessary, in your analysis and calculation, and clearly specify those approximations.**

**180nm technology parameters is used.**

**Minimum Length of NMOS and PMOS is 180nm.**

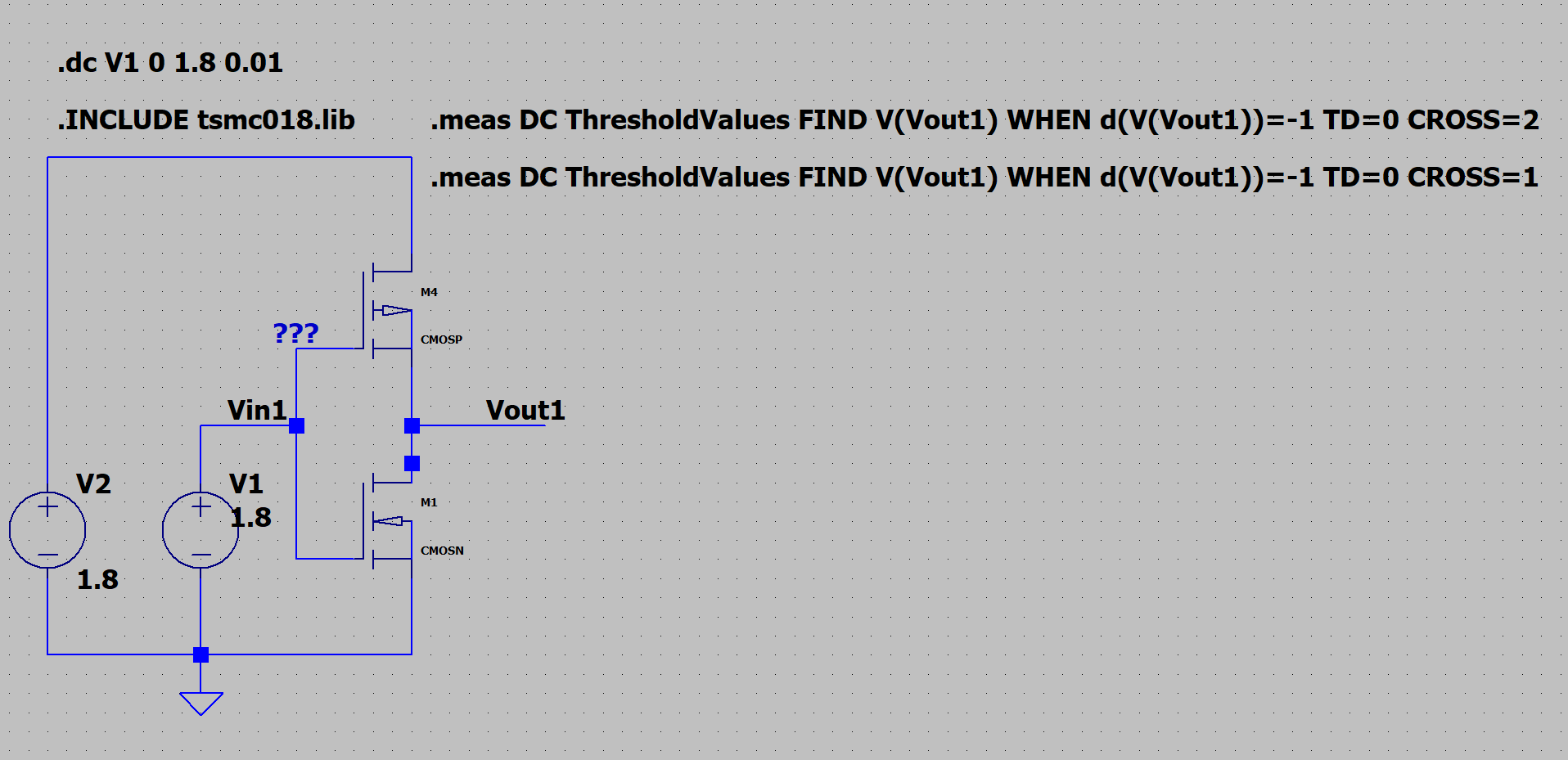
**Minimum Width of NMOS is 400nm.**

**Minimum Width of PMOS is 1280nm for same rise and fall times.**

1. **Simulation of symmetrical and skewed CMOS inverter, and pass transistor:**

**a) Do an analysis to find out the PMOS to NMOS size ratio of the minimum-sized CMOS inverter to have equal rise and fall time. Simulate the static VTC of that inverter, and find out signalling threshold values (VIL, VIH, VOL, VOH) using the slope = –1 criterion from the VTC. Write down high and low noise margins, and the noise immunity of the inverter. Also, simulate the static VTC of an inverter that is sized S times the minimum-sized inverter (both NMOS and PMOS are S times the size of the corresponding NMOS and PMOS of the minimum-sized inverter) for S = 1,2,4, and plot all VTCs in a single graph with clear legends indicating how the sizing affects the VTC.**

**File for Static VTC of the Inverter**: VTC\_CMOS.asc



**Schematic Diagram**

**PMOS to NMOS size ratio = 3.2**

**Threshold Values:**

VIL = 0.709994V, VIH = 0.989723V, VOL = 0.120777V, VOH = 1.66647V

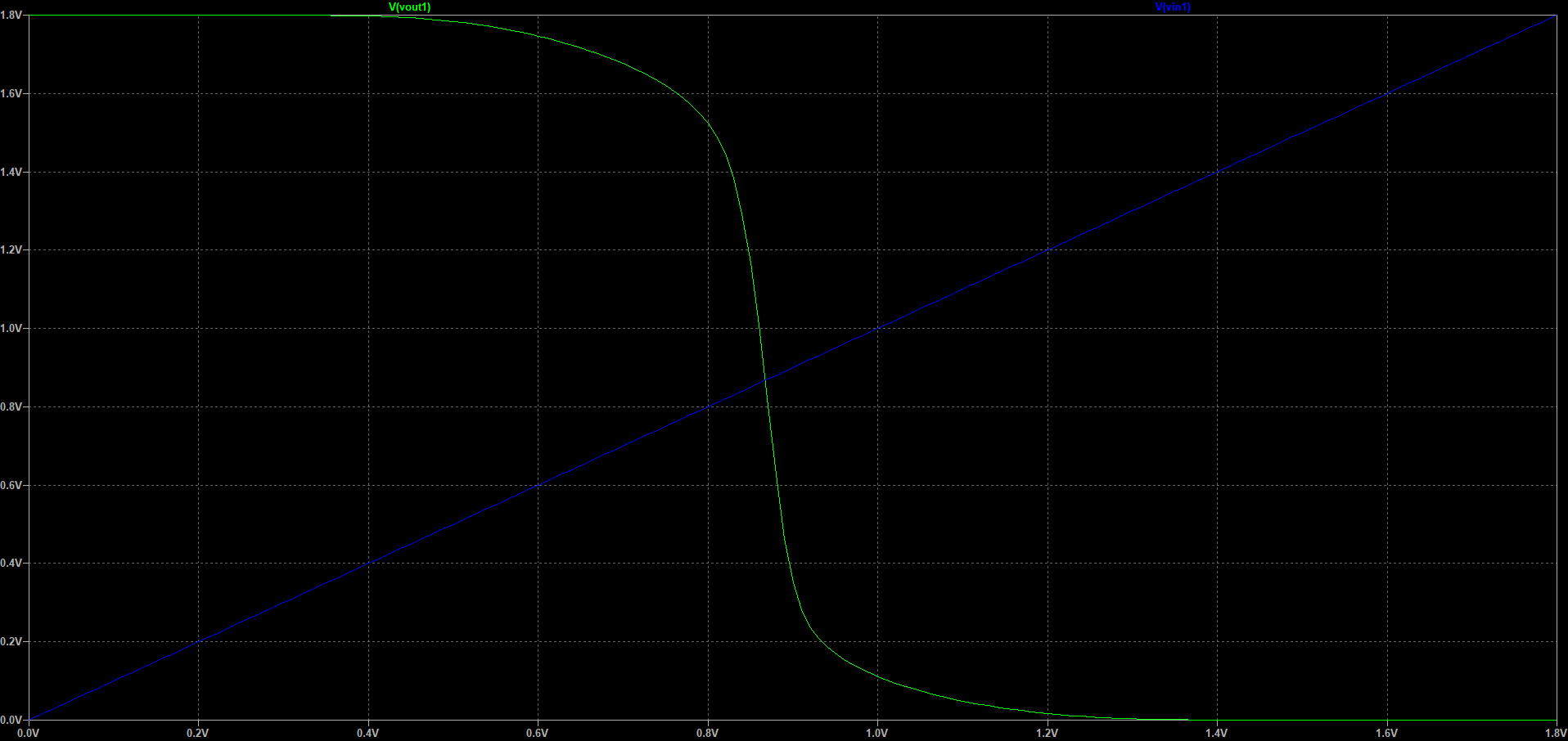
**Noise Margins:**

High Noise Margin: NMH = 0.676747V

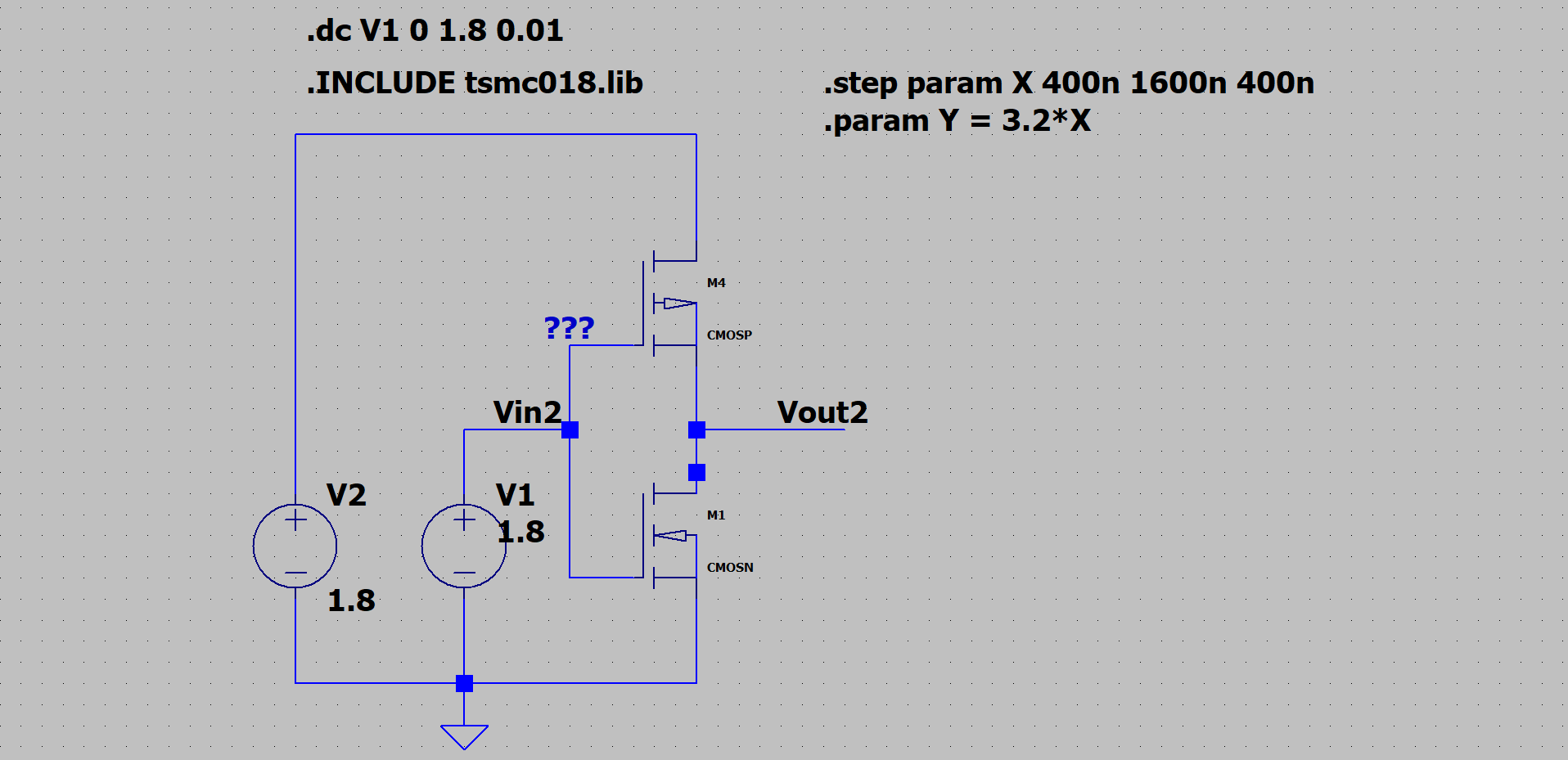
Low Noise Margin: NML = 0.589217V

Noise Immunity: NM = 0.589217V

**Voltage Transfer Characteristics:**

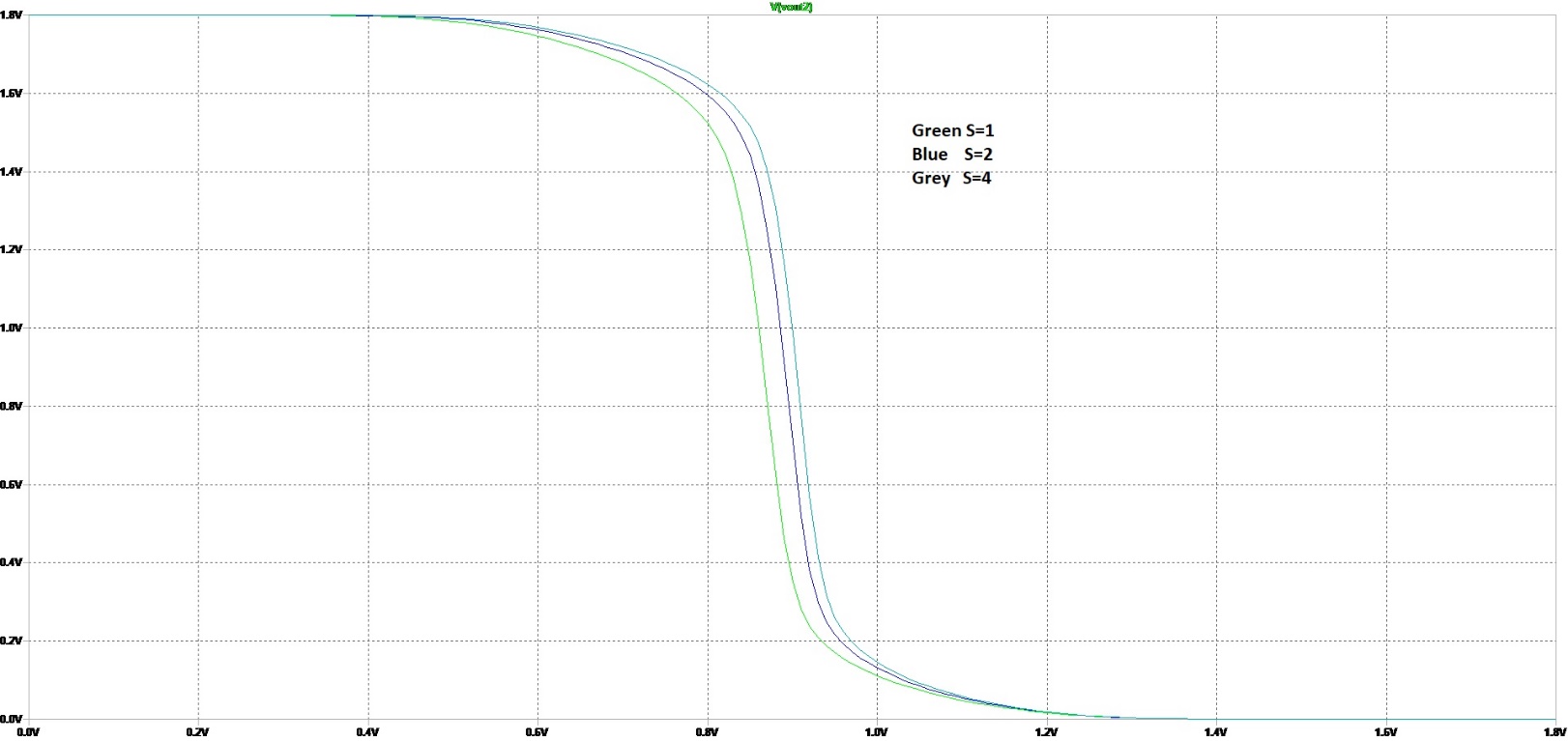


**File for Static VTC of the Inverter that is sized S times the minimum sized inverter**: VTC\_CMOS2.asc



**Schematic Diagram**

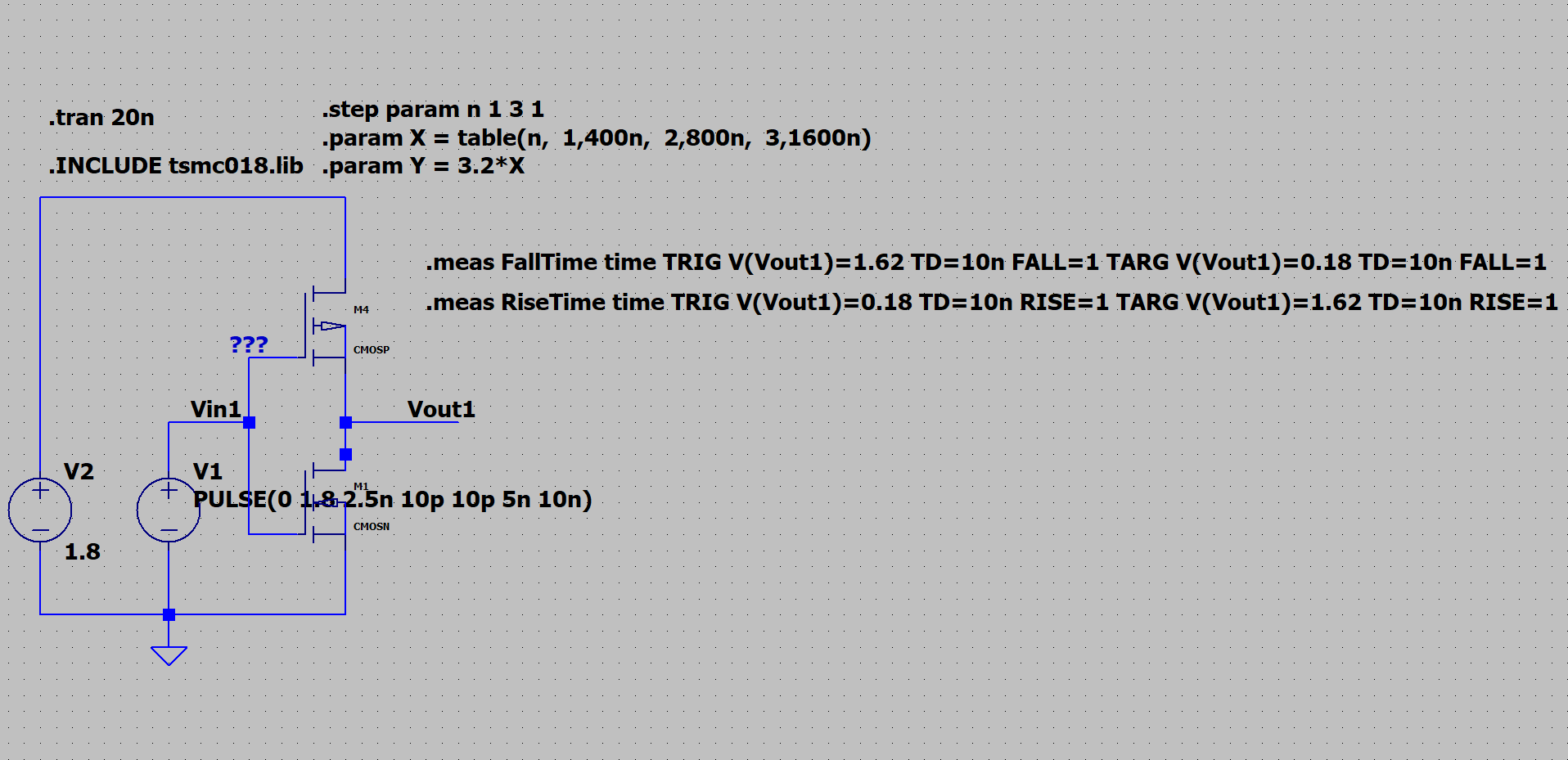
**Voltage Transfer Characteristics:**



**2) Carry out transient analysis to find out the rise time and fall time delays of a CMOS inverter sized S =1,2,4, when (i) no external capacitor is attached, (ii) an external capacitor of 5 pF is attached to the output node. Plot the timing characteristics in a single graph with clearly labelled axes and legends for each value of S and for part (i) and (ii), and tabulate the rise time and fall time delays obtained. Find out the current drawn from the power supply in all cases as the input voltage is swept slowly w.r.t the output, and plot the current vs input voltage in a single graph with clear legends for each value of S and for part (i) and (ii). Calculate and tabulate the static and dynamic power dissipations in all cases, i.e., for each value of S and for part (i) and (ii).**

1. **No external capacitor is attached.**

**File for Simulation**: VTC\_AC\_WITHOUT\_C.asc



**Schematic Diagram**

**Plots:**

A picture containing chart

Description automatically generated

**Fall Time Without C**

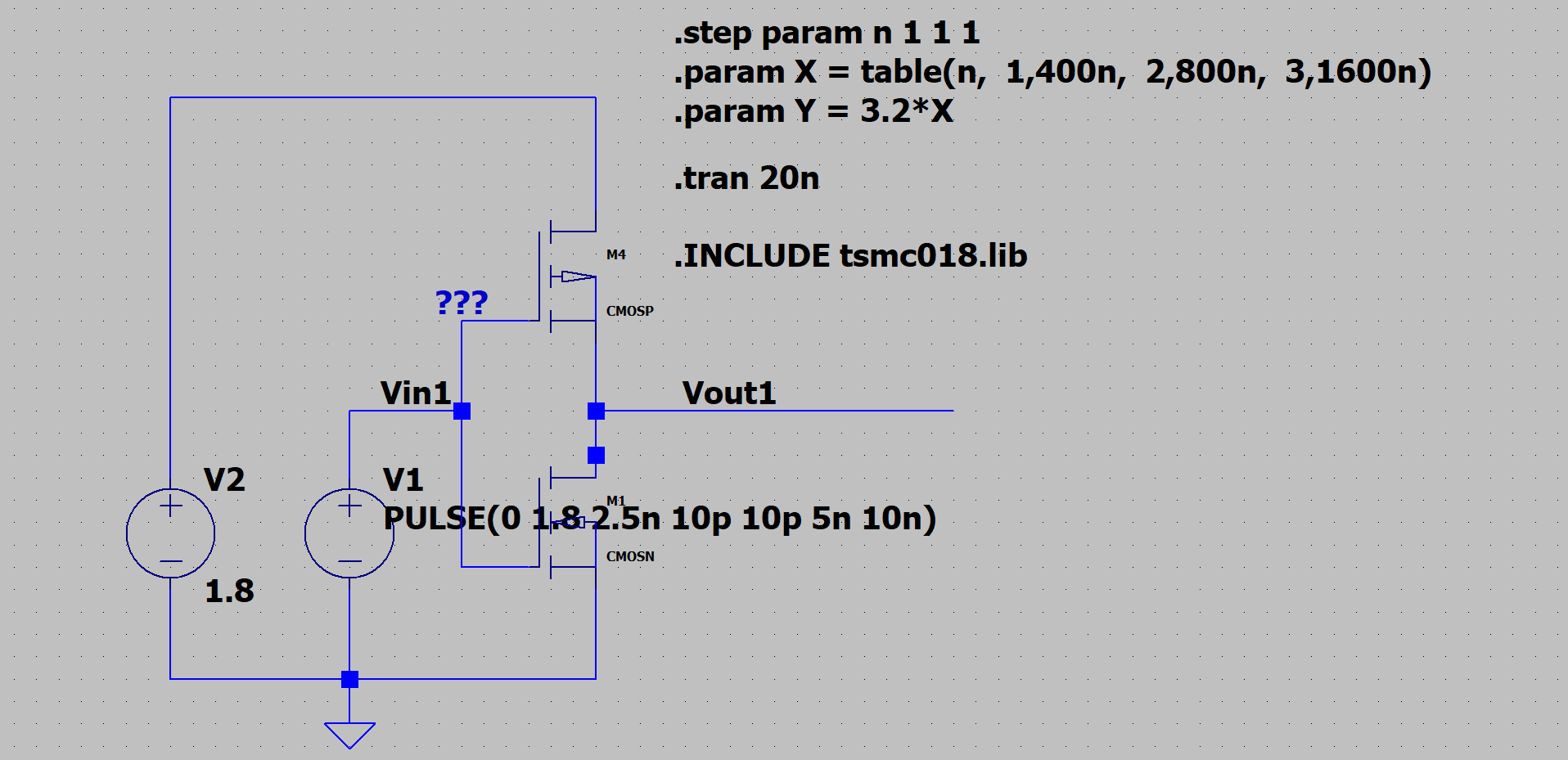
Graphical user interface

Description automatically generated

**Rise Time Without C**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **S=1** | **S=2** | **S=4** |
| **Fall Time** | **9.11ps** | **10.23ps** | **9.22ps** |
| **Rise Time** | **9.33ps** | **8.63ps** | **8.34ps** |

**File for Simulation**: VTC\_CMOS\_CURRENT\_WITHOUT\_C.asc



**Schematic Diagram**

**Plots:**

A screenshot of a computer

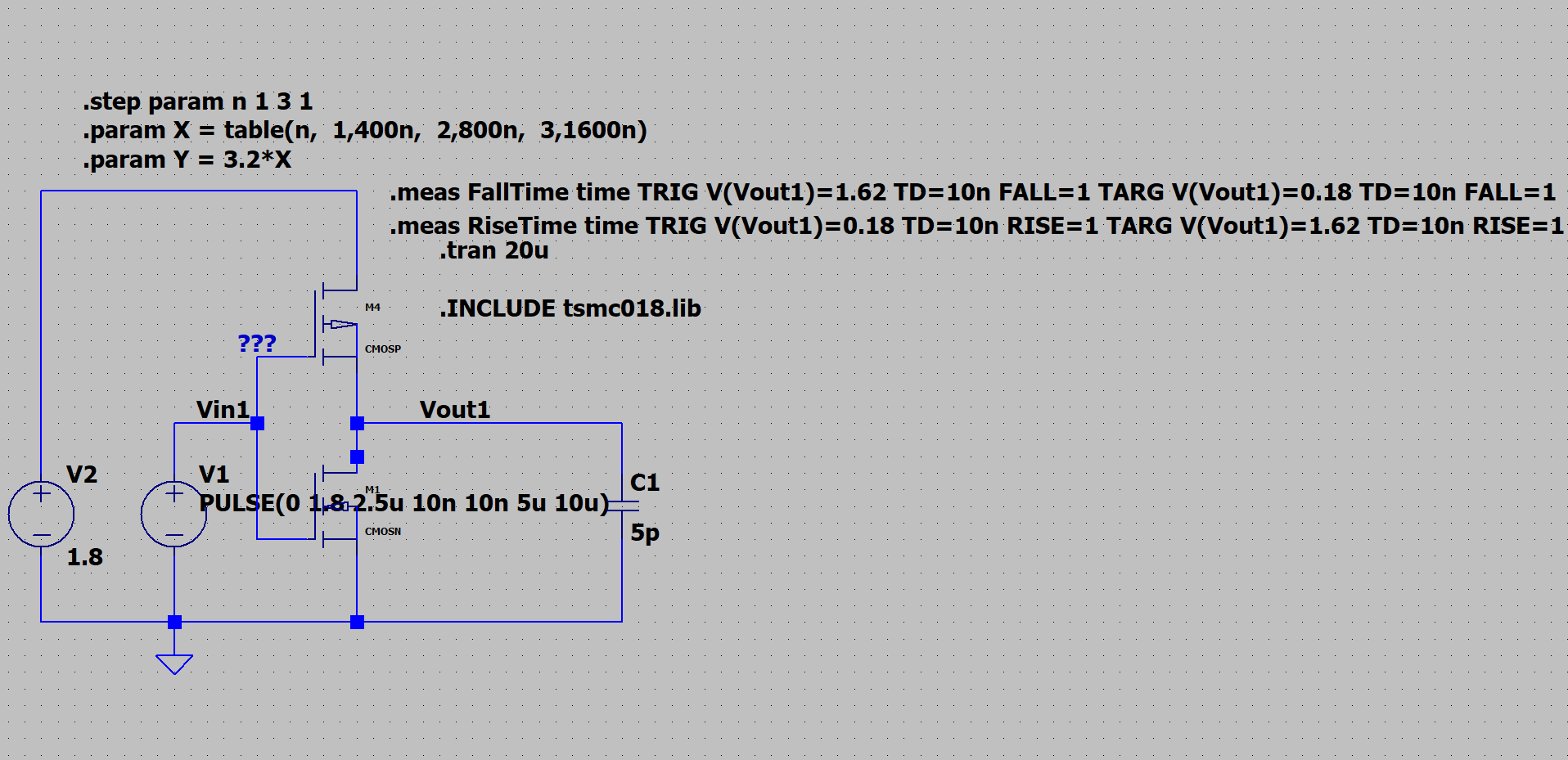
Description automatically generated with medium confidence

**Input Current Without C**

Static Power Dissipation P(steady) = 145pW

1. **An external capacitor of 5pF is attached.**

**File for Simulation**: VTC\_AC\_WITH\_C.asc



**Schematic Diagram**

**Plots:**

Graphical user interface

Description automatically generated

**Fall Time With C**

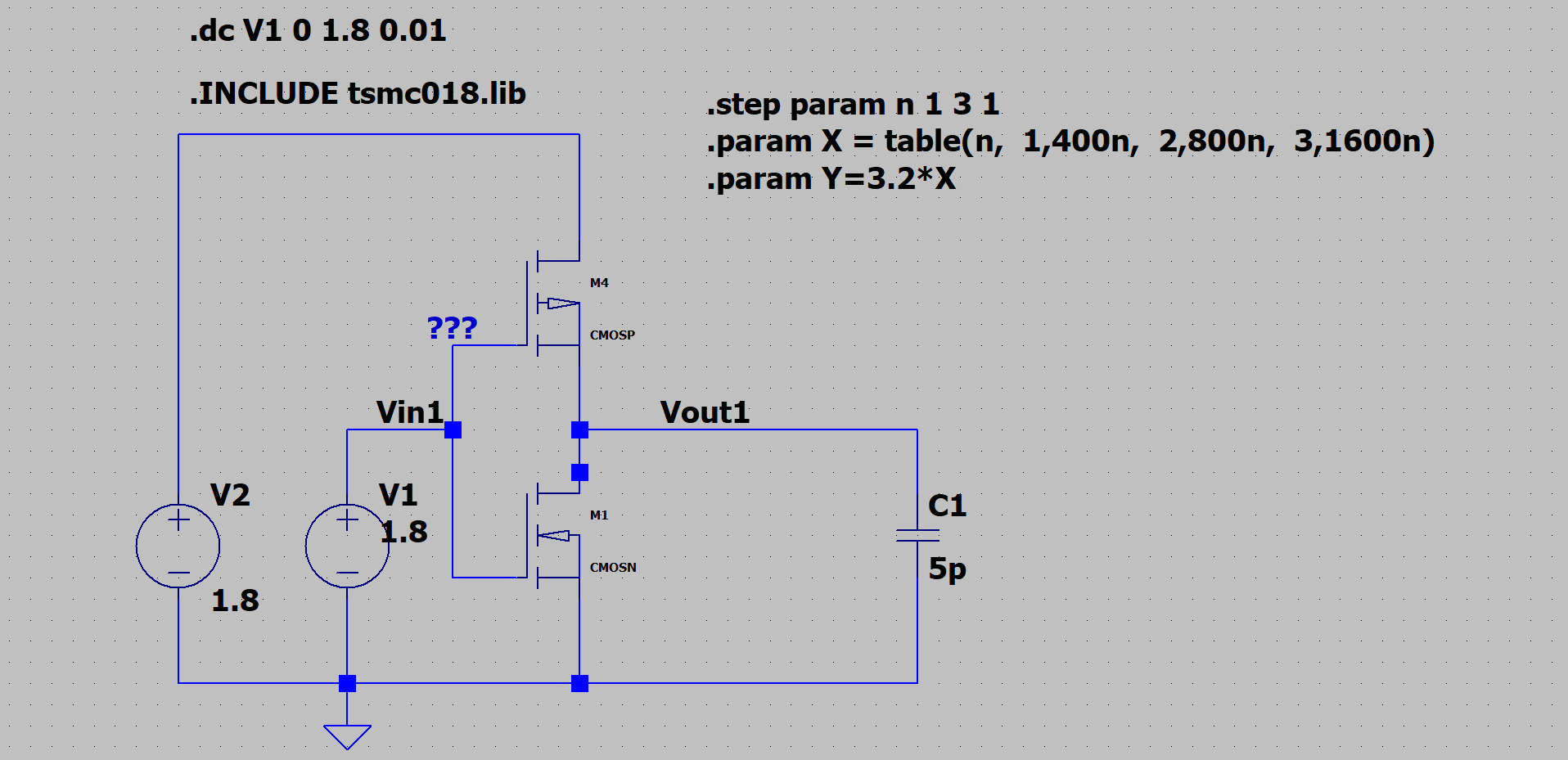
Graphical user interface, application

Description automatically generated

**Rise Time With C**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **S=1** | **S=2** | **S=4** |
| **Fall Time** | **30.04ns** | **17.38ns** | **9.92ns** |
| **Rise Time** | **30.03ns** | **16.64ns** | **8.74ns** |

**File for Simulation**: VTC\_CMOS\_CURRENT\_WITH\_C.asc



**Schematic Diagram**

**Plots:**

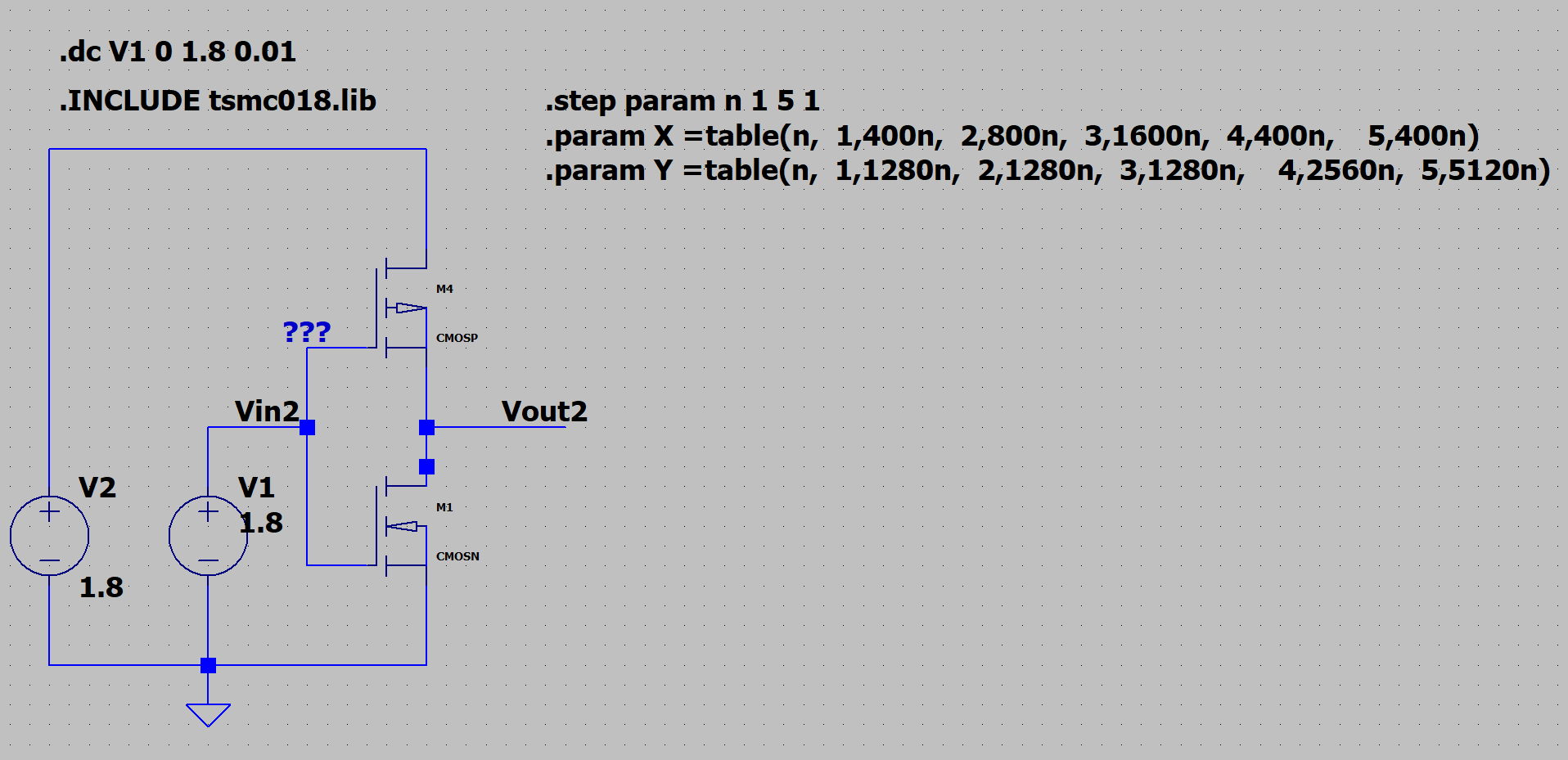
Chart

Description automatically generated

**Input Current With C**

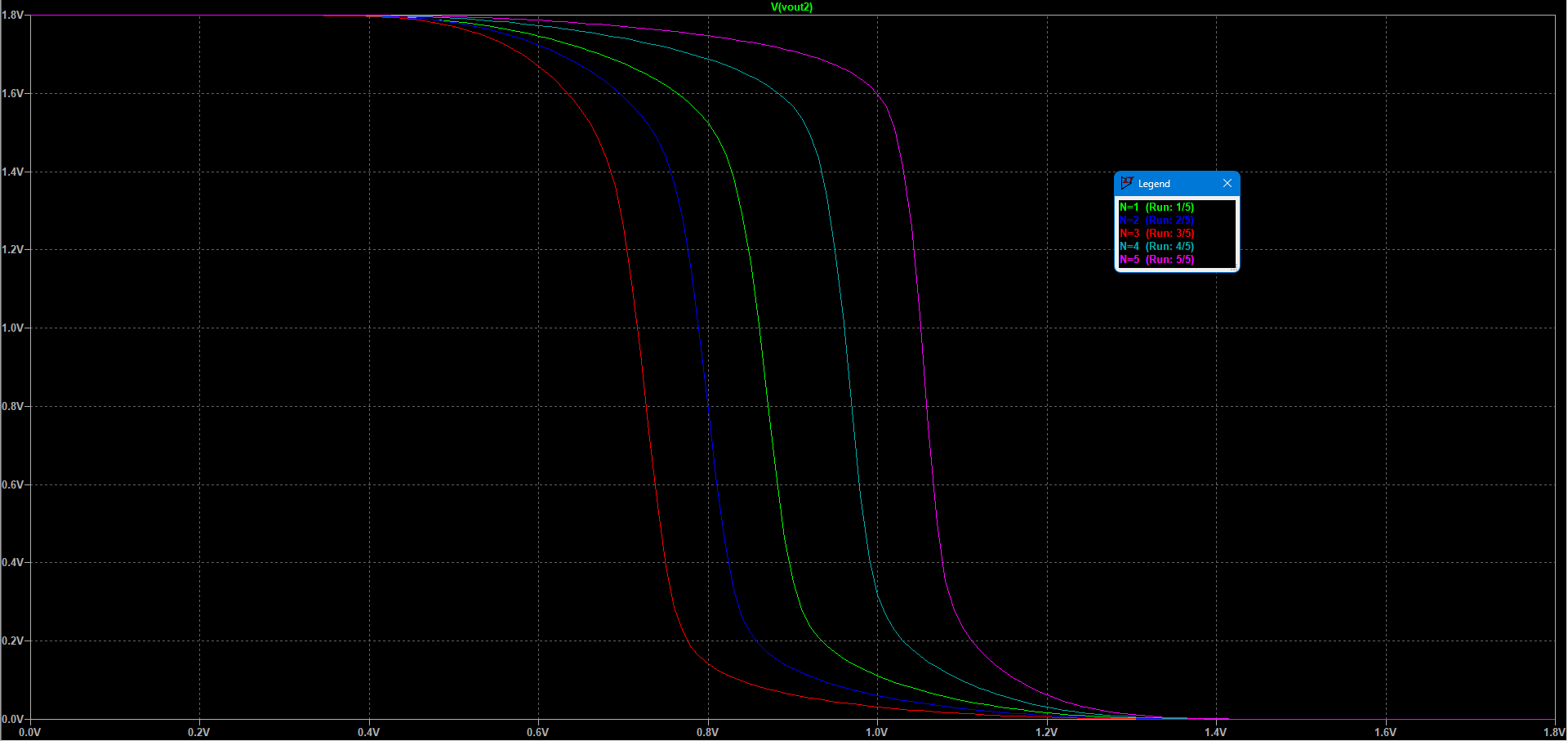
**3) Simulate the static VTC of an inverter in which the NMOS is sized Kn times the size of the corresponding NMOS of the minimum-sized inverter for Kn = 1,2,4, keeping the size of the PMOS the same as that of the corresponding PMOS of the minimum-sized inverter. Similarly, simulate the static VTC of an inverter in which the PMOS is sized Kp times the size of the corresponding PMOS of the minimum-sized inverter for Kp = 1,2,4, keeping the size of the NMOS the same as that of the corresponding NMOS of the minimum-sized inverter. Plot all these VTCs in a single graph with clear legends indicating how sizing of skewed CMOS inverter affects the VTC.**

**File for Simulation**: VTC\_CMOS2\_1C.asc



**Schematic Diagram**

**Plots:**

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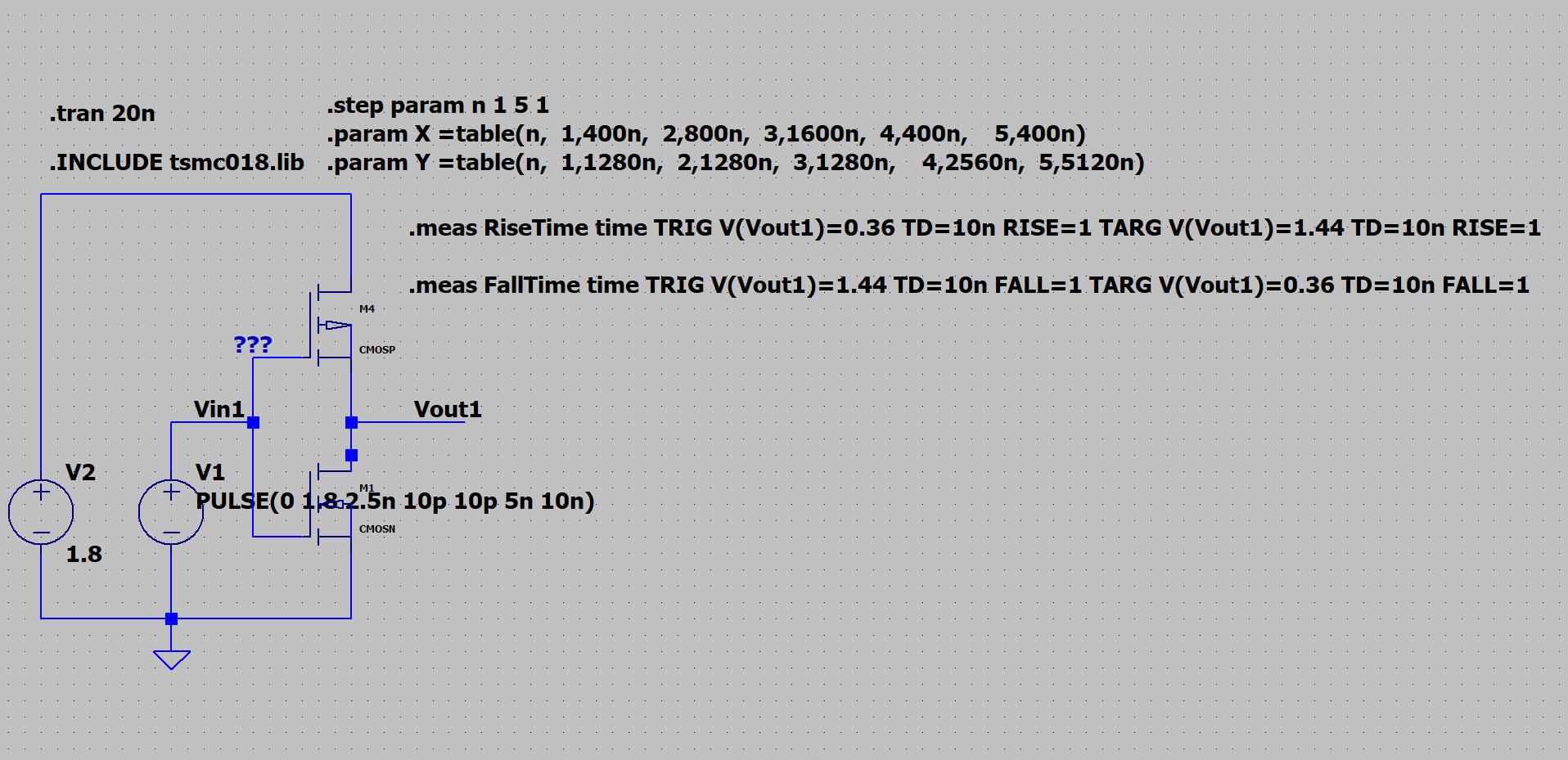
**Voltage Transfer Characteristics**

|  |  |  |  |
| --- | --- | --- | --- |
| **N** | **NMOS WIDTH** | **PMOS WIDTH** | **COLOUR** |
| **1** | **400nm** | **1280nm** | **GREEN** |
| **2** | **800nm** | **1280nm** | **BLUE** |
| **3** | **1600nm** | **1280nm** | **RED** |
| **4** | **400nm** | **2560nm** | **GREY** |
| **5** | **400nm** | **5120nm** | **PURPLE** |

**4) Carry out transient analysis to find out the rise time and fall time delays in each case when (i) no external capacitor is attached, (ii) an external capacitor of 5 pF is attached to the output node. Plot the timing characteristics in a single graph with clearly labelled axes and legends for each case and for part (i) and (ii), and tabulate the rise time and fall time delays obtained. Also, find out the current drawn from the power supply in all cases as the input voltage is swept slowly w.r.t the output, and plot the current vs input voltage in a single graph with clear legends for each case and for part (i) and (ii). Calculate and tabulate the static and dynamic power dissipations in all cases.**

1. **No external capacitor is attached.**

**File for Simulation**: 1D\_VTC\_AC\_WITHOUT\_C.asc



**Schematic Diagram**

**Plots:**

A picture containing chart

Description automatically generated

**Fall Time Without C**

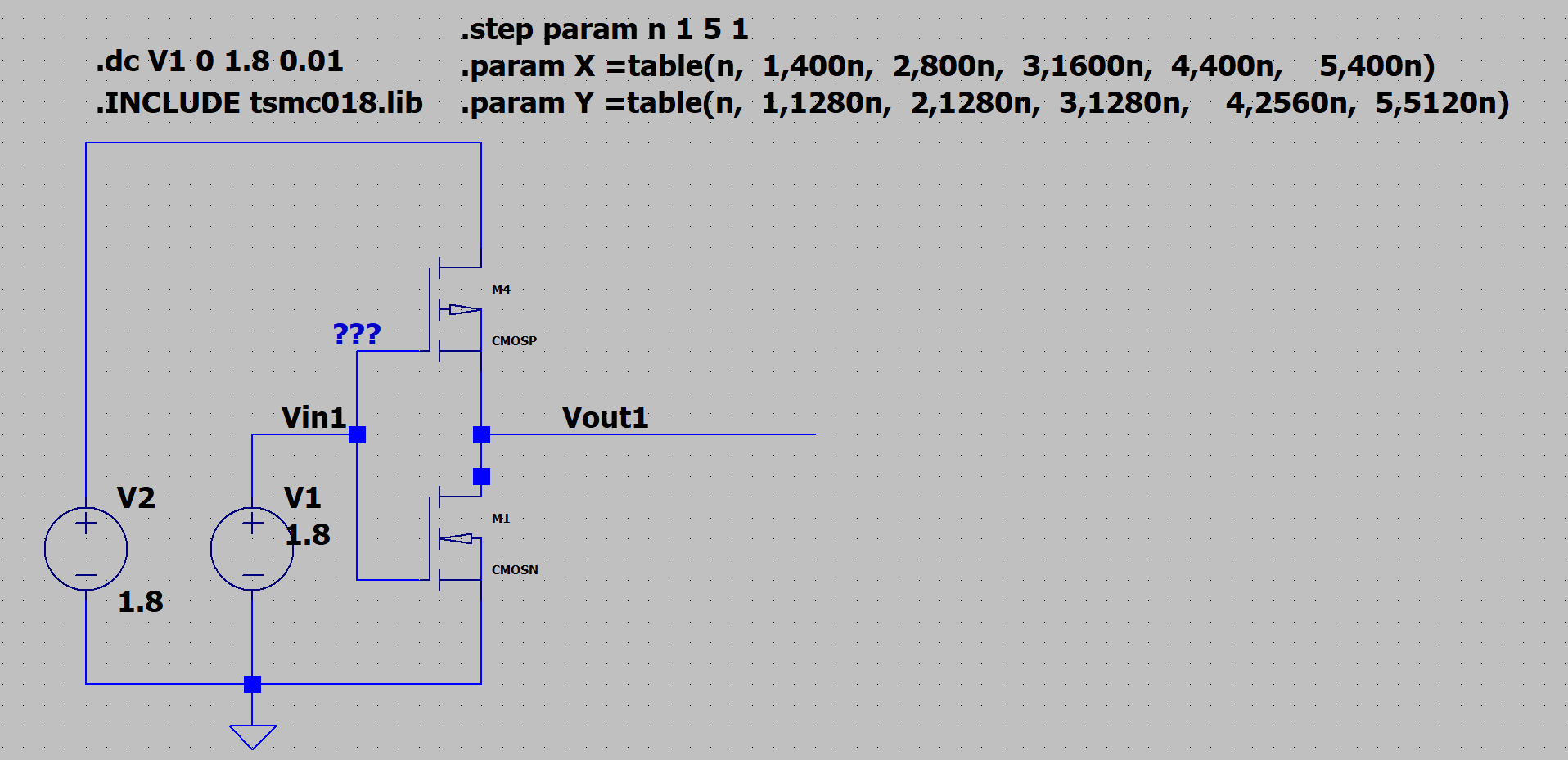
Graphical user interface

Description automatically generated with medium confidence

**Rise Time Without C**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  | **NMOS SIZING** | | **PMOS SIZING** | |
| **COLOUR** | **GREEN** | **BLUE** | **RED** | **GREY** | **PURPLE** |
|  | **S=1** | **S=2** | **S=4** | **S=2** | **S=4** |
| **Fall Time** | **6.64ps** | **4.94ps** | **3.56ps** | **9.79ps** | **16.58ps** |
| **Rise Time** | **6.28ps** | **7.32ps** | **10.30ps** | **4.73ps** | **4.40ps** |

**File for Simulation**: 1D\_VTC\_CMOS\_CURRENT\_WITHOUT\_C.asc



**Schematic Diagram**

**Plots:**

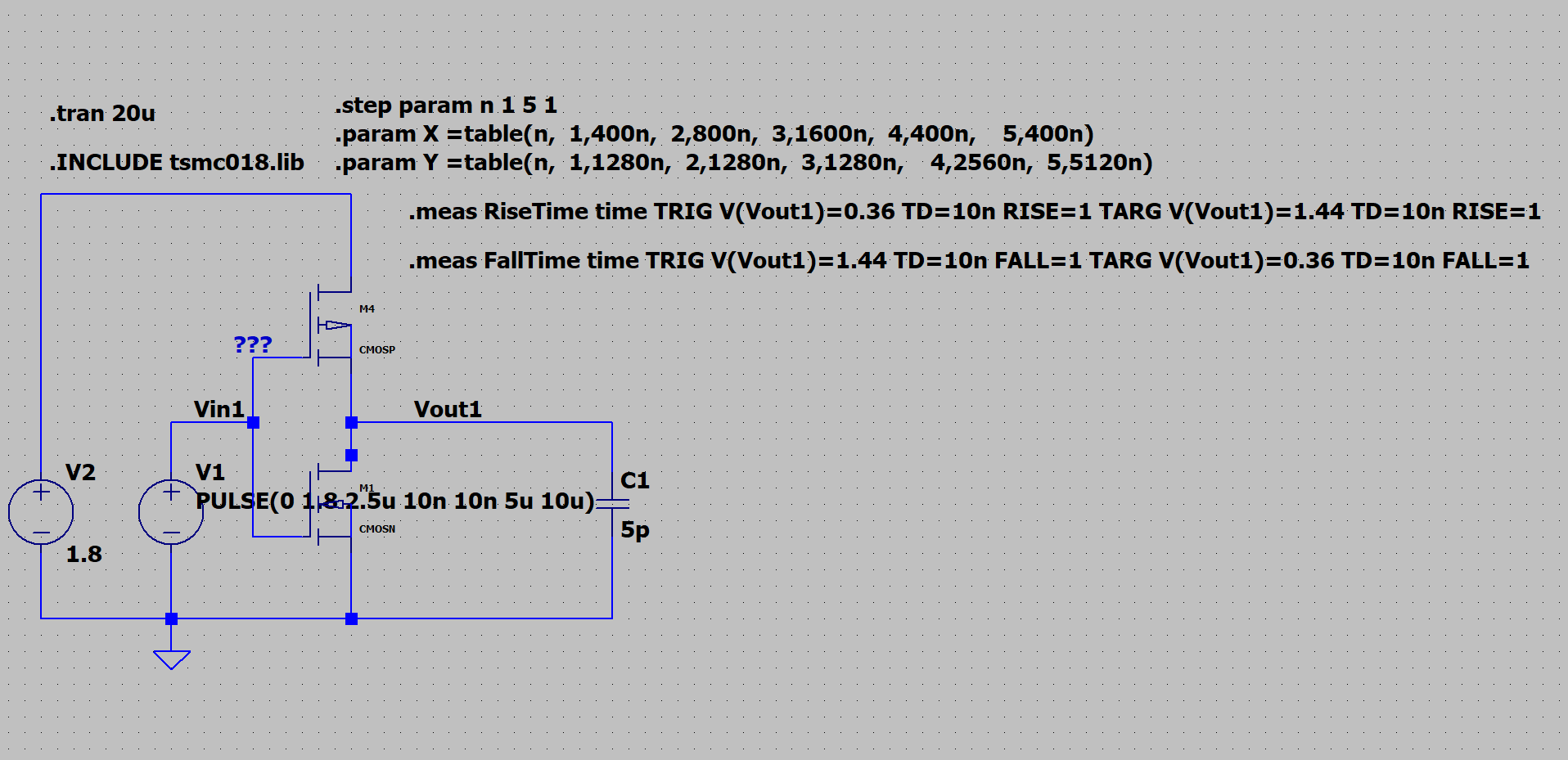
A screenshot of a computer

Description automatically generated with medium confidence

**Input Current Without C**

1. **An external capacitor of 5pF is attached.**

**File for Simulation**: 1D\_VTC\_AC\_WITH\_C.asc



**Schematic Diagram**

**Plots:**

Graphical user interface

Description automatically generated

**Fall Time With C**

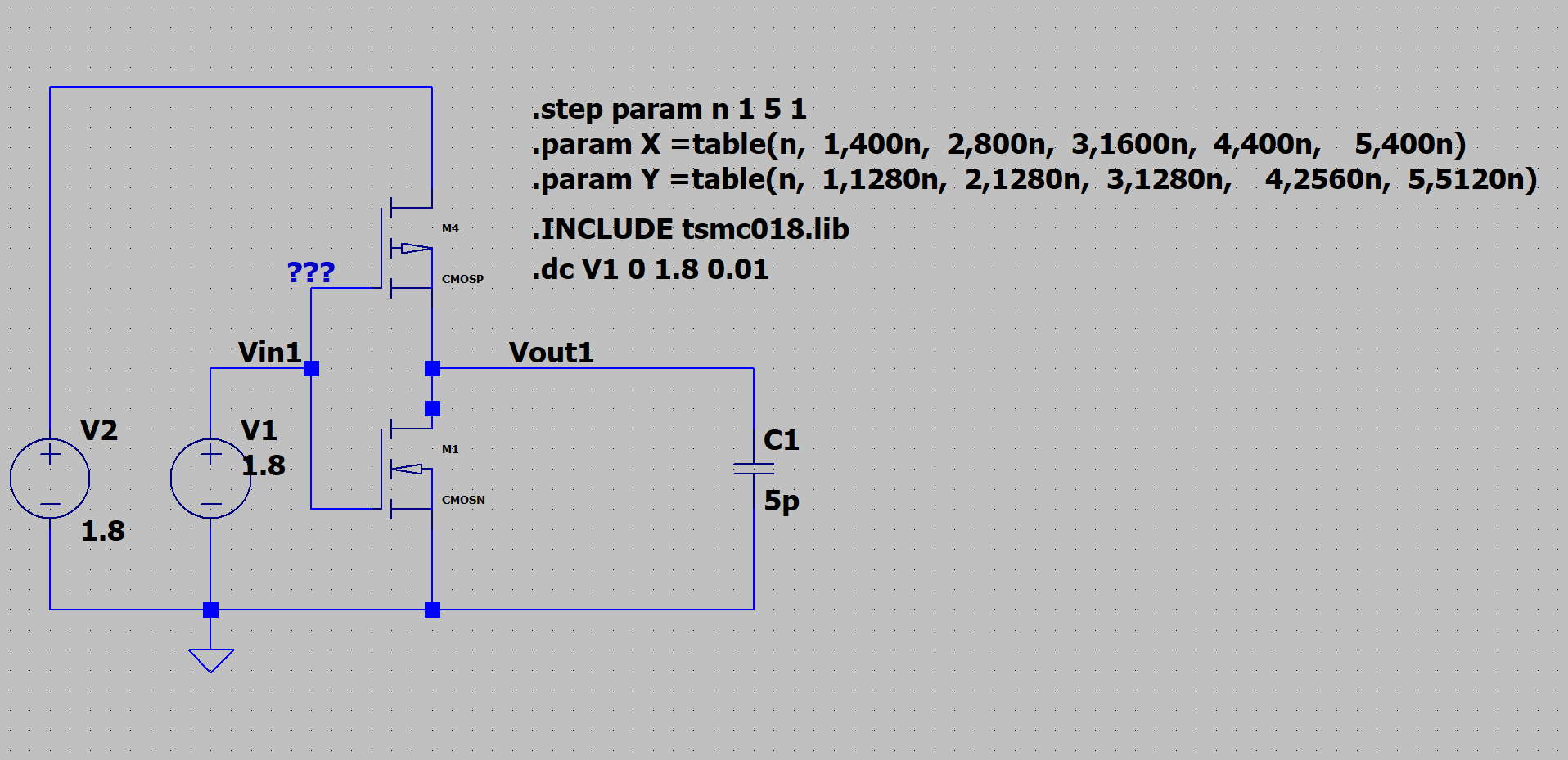
Graphical user interface

Description automatically generated

**Rise Time With C**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  | **NMOS SIZING** | | **PMOS SIZING** | |
| **COLOUR** | **GREEN** | **BLUE** | **RED** | **GREY** | **PURPLE** |
|  | **S=1** | **S=2** | **S=4** | **S=2** | **S=4** |
| **Fall Time** | **21.15ns** | **11.90ns** | **6.71ns** | **20.86ns** | **20.69ns** |
| **Rise Time** | **20.27ns** | **20.40ns** | **20.46ns** | **10.44ns** | **5.67ns** |

**File for Simulation**:1D\_ VTC\_CMOS\_CURRENT\_WITH\_C.asc



**Schematic Diagram**

**Plots:**

A screenshot of a computer

Description automatically generated with medium confidence

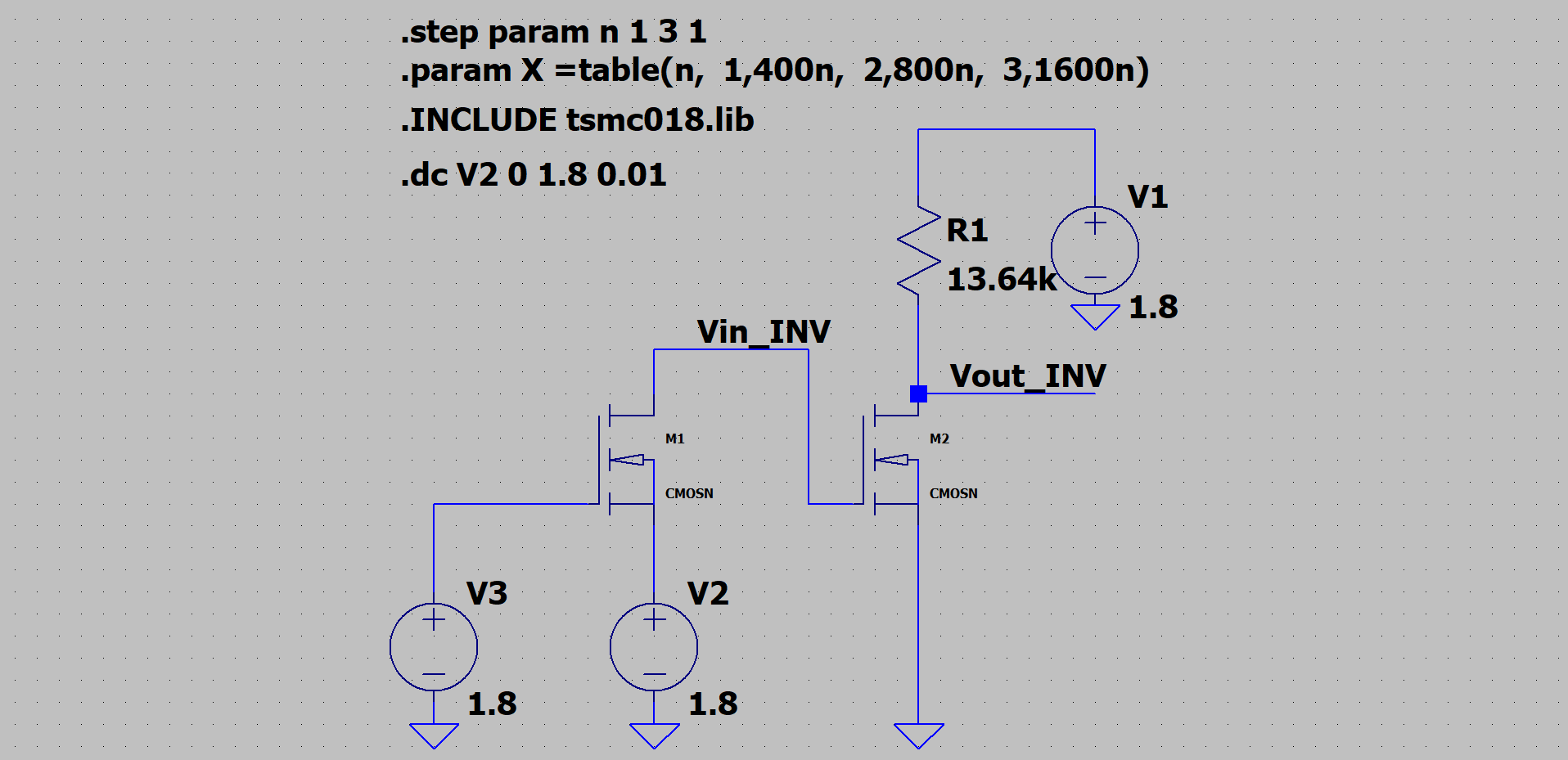
**Input Current With C**

**5) Create a circuit consisting of a NMOS pass transistor having size Kn=1,2,4, driving an NMOS inverter of minimum size connected to the source/drain of the NMOS pass transistor (choose the resistor value in the NMOS inverter to have equal rise and fall times which also should be equal to that of a minimum-sized symmetrical CMOS inverter).**

For the minimum sizing and equal rise and fall times, Resistance is taken as 13.64kΩ.

**Apply an input signal to the source/drain of the NMOS pass transistor of which the gate is connected to VDD, and plot the voltage waveform at the input and output of the inverter and tabulate the delay at both the input and output of the inverter for all values of Kn, when the input signal varies slowly from (i) low to high, (ii) high to low. From these results, plot the resistance of the pass transistor vs input voltage in a single graph with clearly labelled axes and legends for all values of Kn.**

**For Drain Input Voltage from Low to High**



**Schematic Diagram**

**Plots:**

**Chart

Description automatically generated**

**Inverter Input Voltage**

**Chart

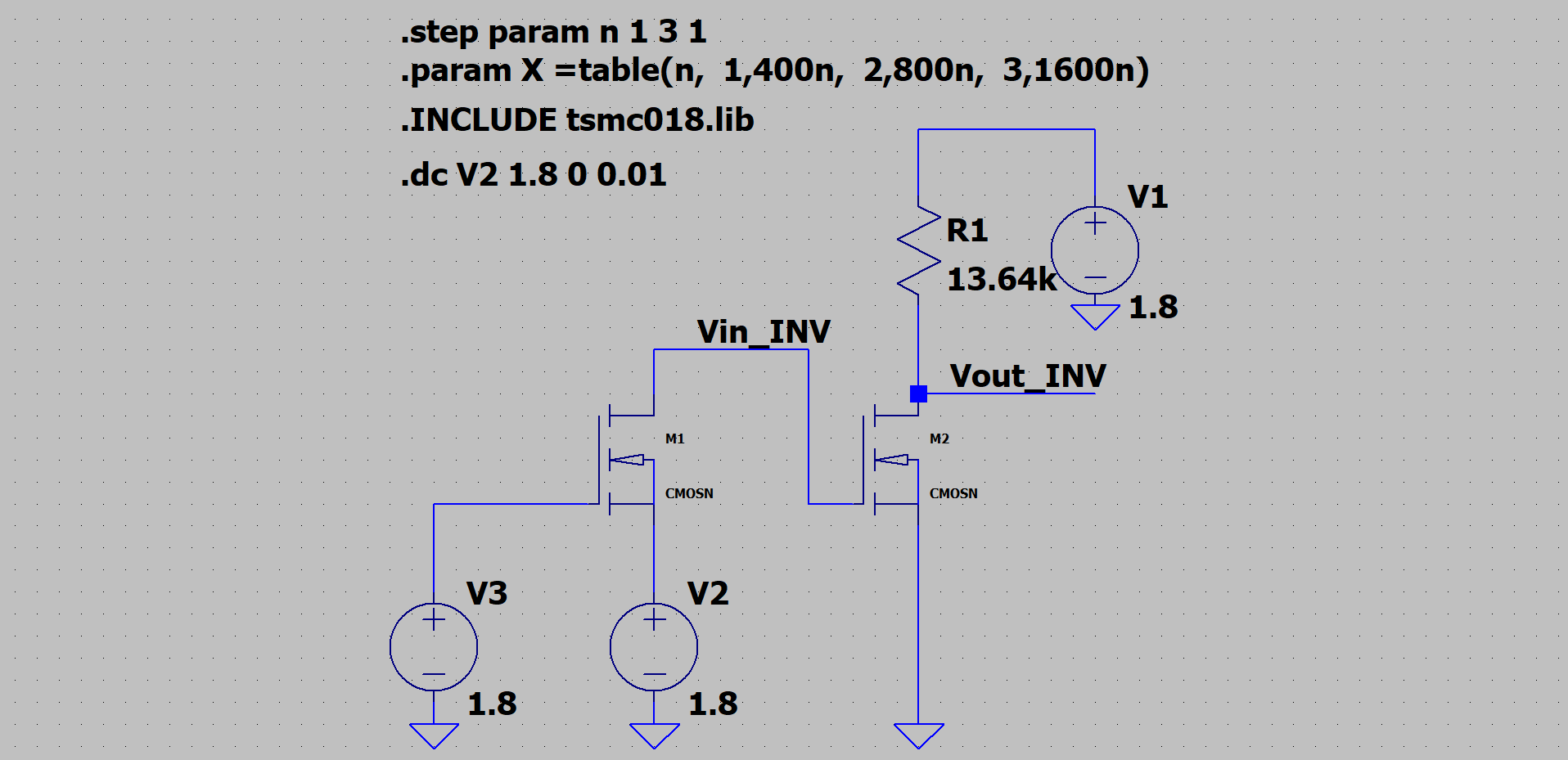
Description automatically generated with medium confidence**

**Inverter Output Voltage**

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**Pass Transistor Resistance**

**For Drain Input Voltage from High to Low**



**Schematic Diagram**

**Plots:**

**Graphical user interface

Description automatically generated**

**Inverter Input Voltage**

**Graphical user interface

Description automatically generated**

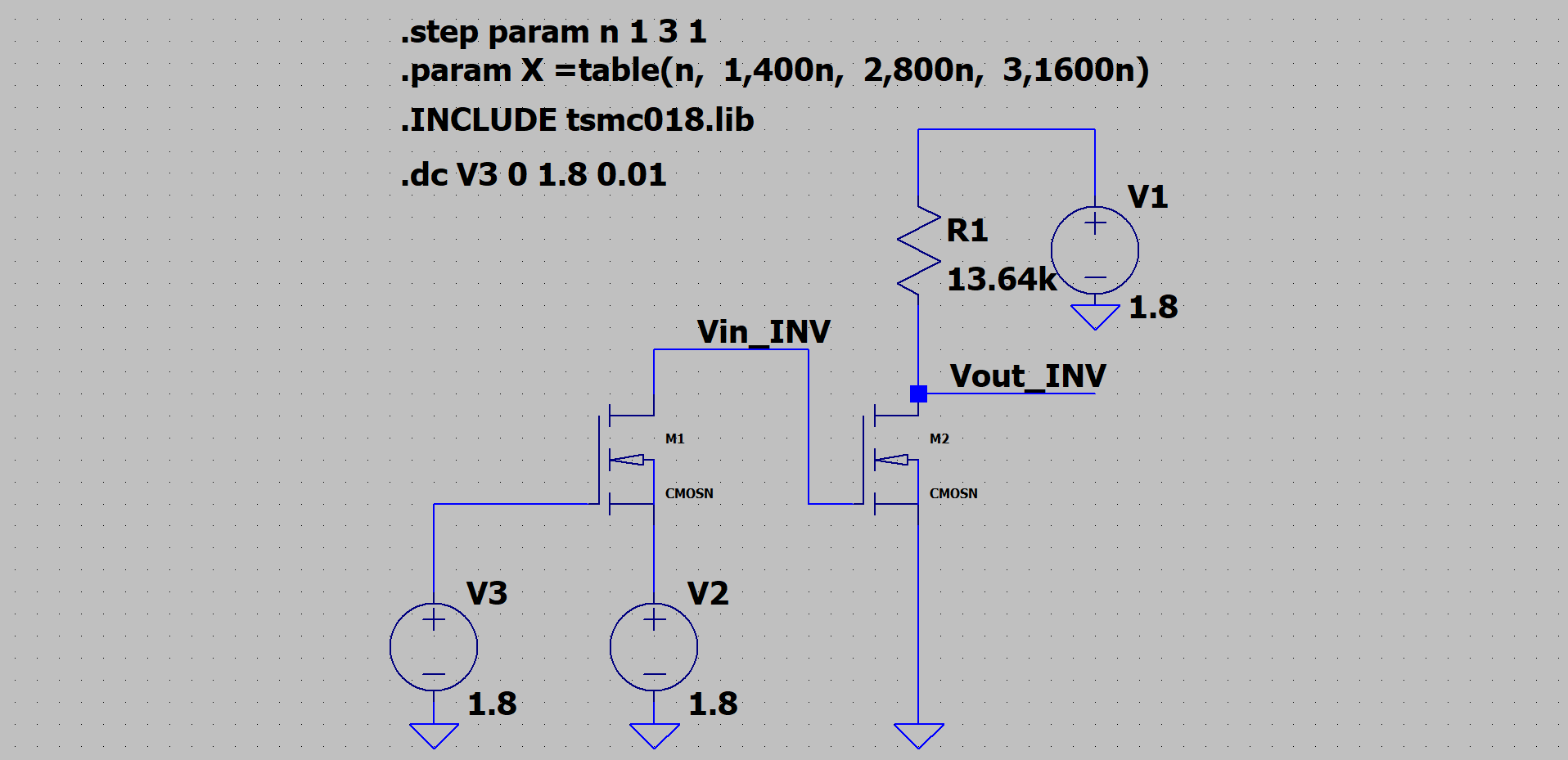
**Inverter Output Voltage**

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**Pass Transistor Resistance**

**Do another simulation to plot the voltage waveform at the input and output of the inverter and tabulate the delay at both the input and output of the inverter for all values of Kn, when the source/drain of the NMOS pass transistor is connected to VDD and the input signal which is applied to the gate of the NMOS pass transistor varies slowly from (i) low to high, (ii) high to low. From these results, plot the resistance of the pass transistor vs input voltage in a single graph with clearly labelled axes and legends for all values of Kn.**

**For Gate Input Voltage from Low to High**



**Schematic Diagram**

**Plots:**

**Graphical user interface

Description automatically generated**

**Inverter Input Voltage**

**A picture containing chart

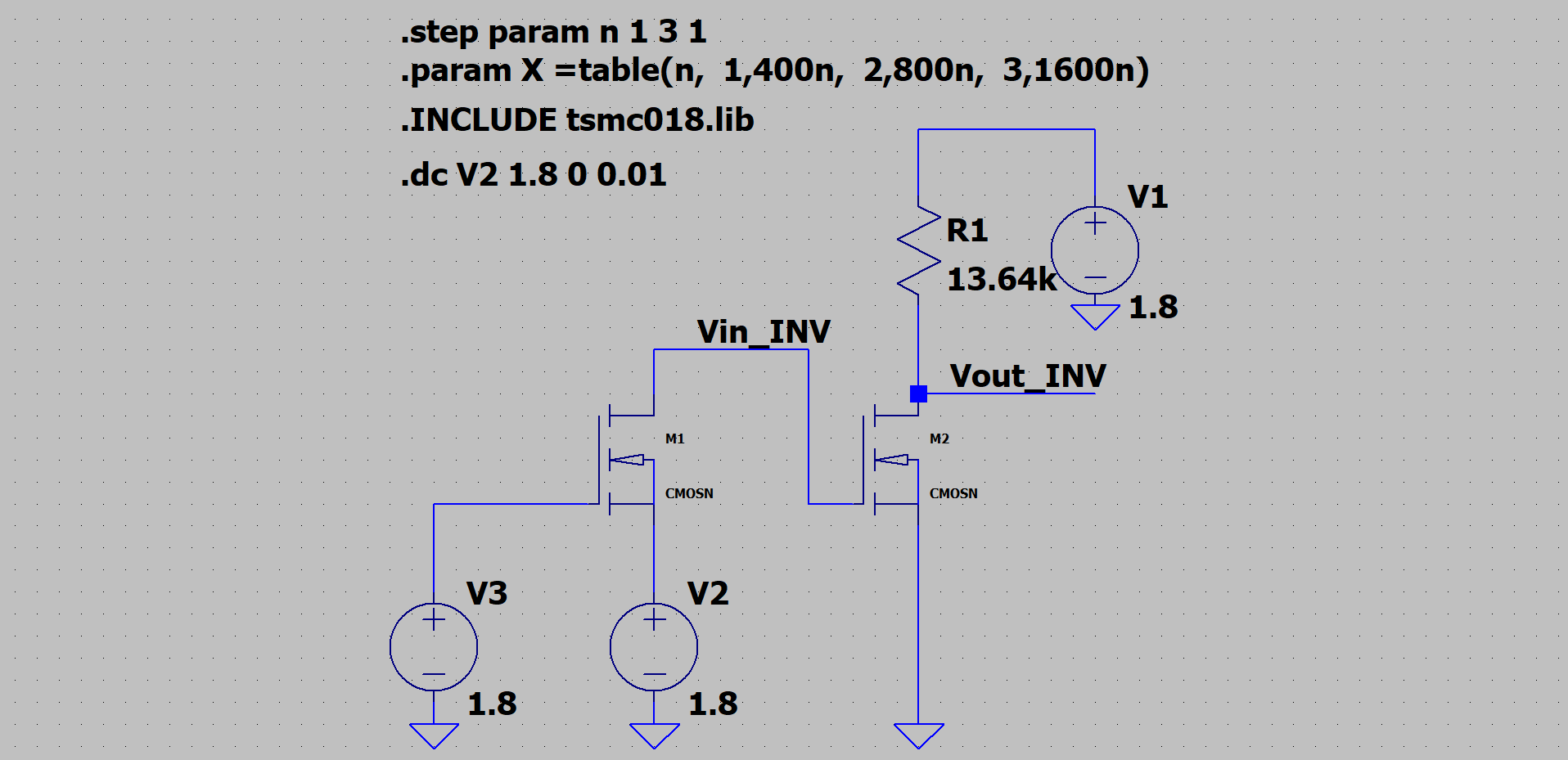
Description automatically generated**

**Inverter Output Voltage**

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**Pass Transistor Resistance**

**For Gate Input Voltage from High to Low**



**Schematic Diagram**

**Plots:**

**Graphical user interface

Description automatically generated**

**Inverter Input Voltage**

**Chart

Description automatically generated with low confidence**

**Inverter Output Voltage**

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**Pass Transistor Resistance**